

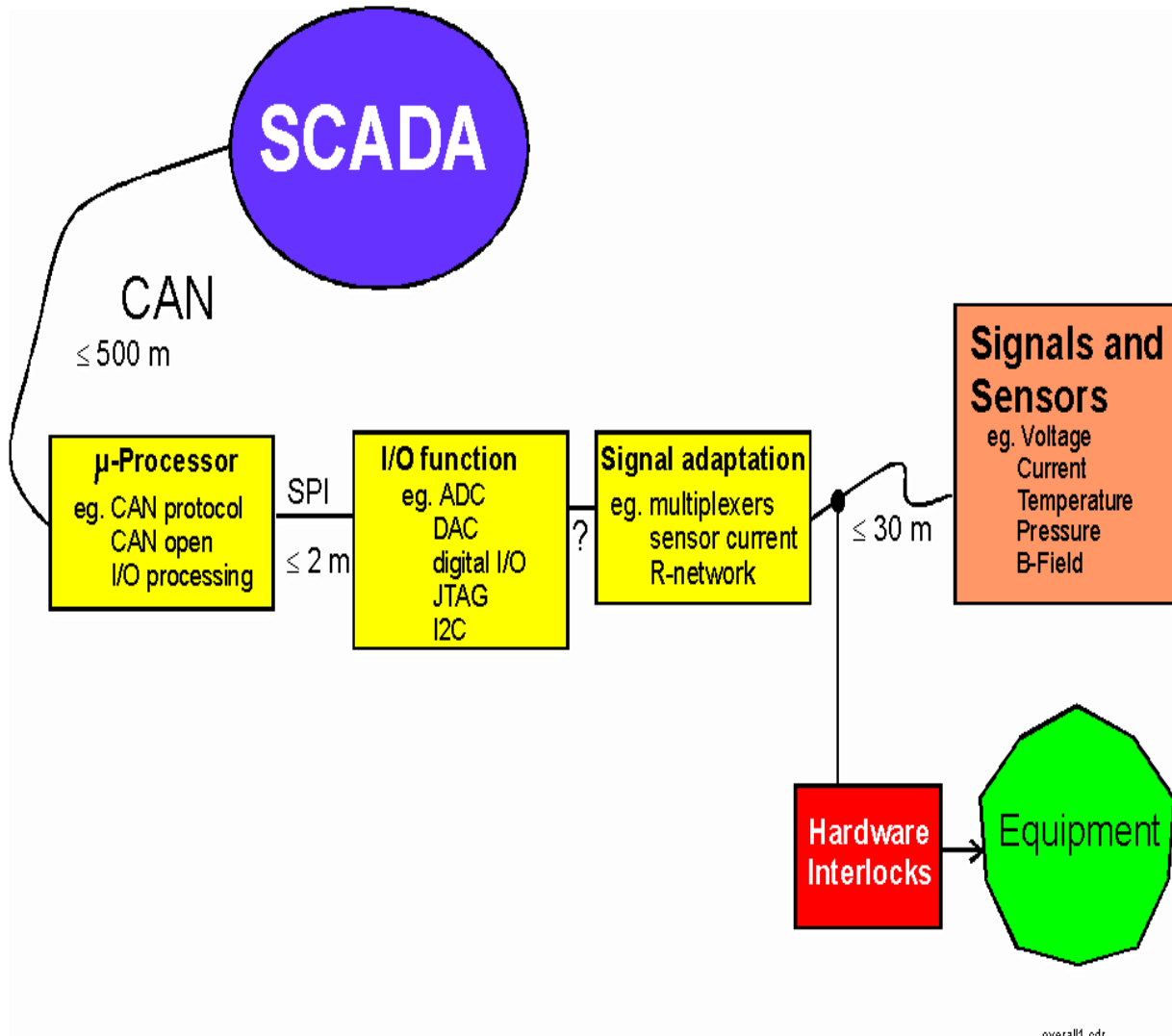
# Pixel DCS Status and Issues 2/ 2001

G. D. Hallewell: RAL/CPPM

## Contents

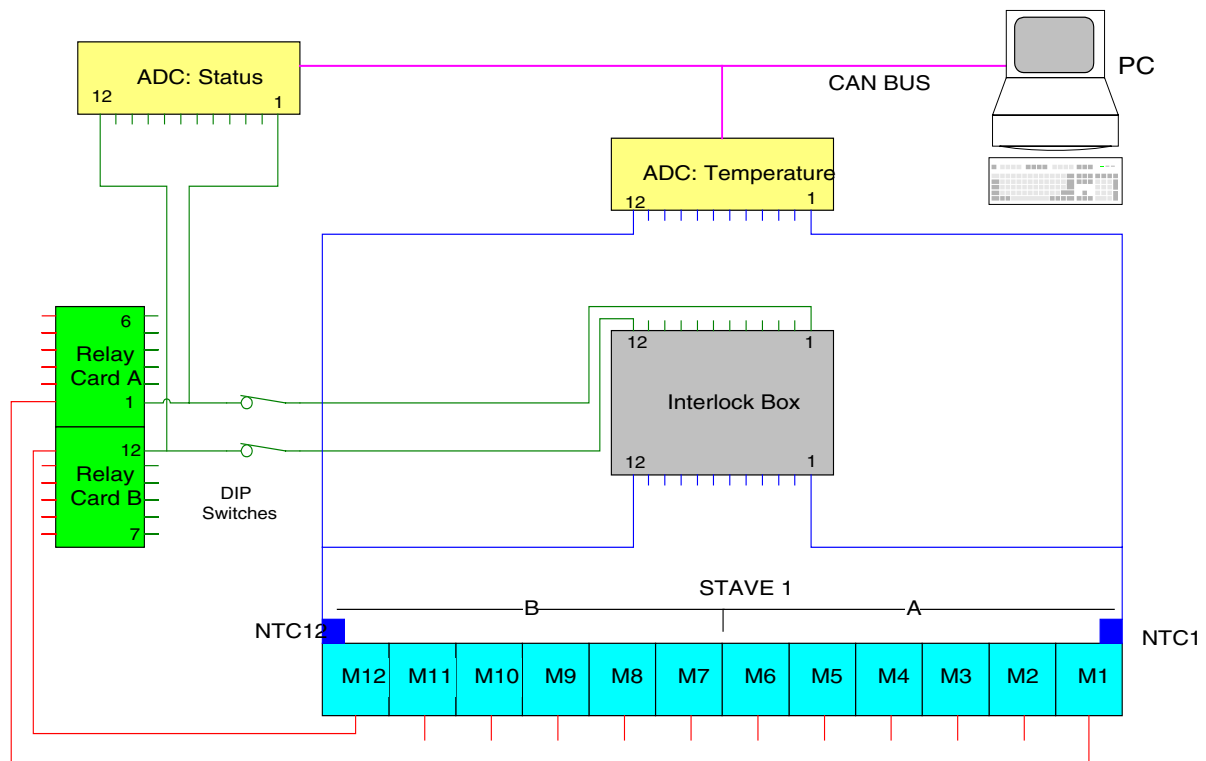
- **On-module NTC Temperature sensors & I-boxes (Interlock Boxes) to protect Pixel Modules**
- **Flow and Pressure Control in the Evaporative Cooling System and Analog Pneumatic Controls Development**
- **The “Embedded Local Monitor Box (E-LMB) as an acquisition node for slow monitoring.**
- **Possible Sharing of NTC information with LMBs for independent logging (connectivity issues)**
- **An Add-On DAC for the E-LMB (Draft Specification)**
- **Numbers of E-LMBs (and signal adapters) in final system for module temperature, PID flow control & PID tube bundle temperature control**
- **First Experience with PVSS2 (final SCADA) software.**
- **Highly Redundant LV UPS for I-Box, controls power**
- **Where from here/ how to divide the work**

# Major Elements (Hard & Soft) of the Detector Control System



# On-module NTC Temperature sensors & I-boxes (Interlock Boxes) to protect Pixel Modules

## Interlock Box Control System



## NTC Thermal Sensors glued on 22 Modules of Geneva Barrel SCT Full Length Prototype (Semitec AT series: 10kW @ 25 C)

NTC SMD resistors (Taiyo Yuden & Semitec) irradiated to  
 $1.2 \times 10^{15} \text{ p (25 GeV/c) /cm}^2$ .

Dispersion pre&post irradiation  $\sim 0.3\text{K}$ , ( $< 0.5 \text{ K OK}$ )

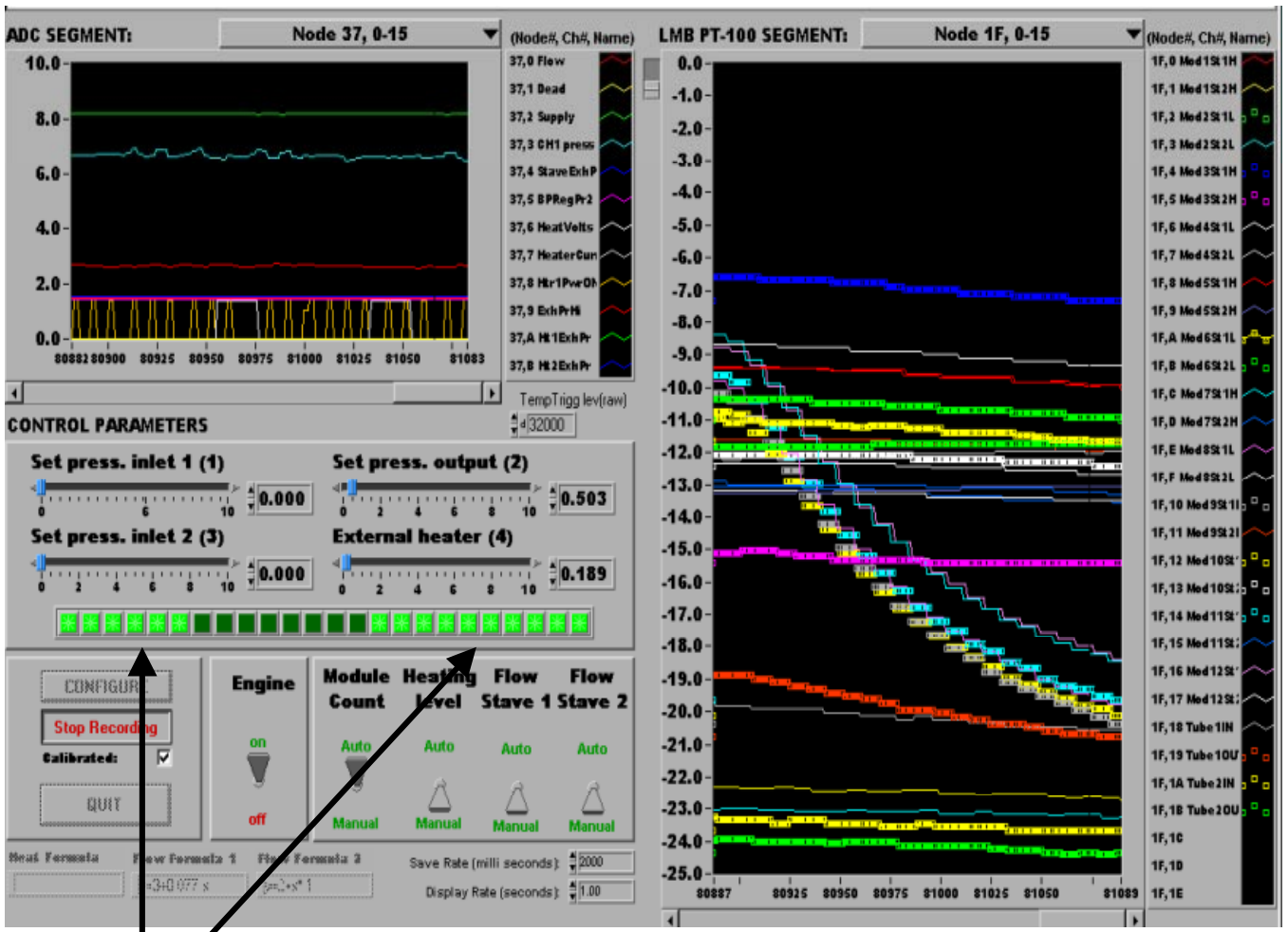
## I-Box Hysteresis

In PIXELS, interlock set (“POWER DISABLE”) @  $0.15^\circ\text{C}$   
and reset (“POWER RE-ENABLE”) @  $-0.79^\circ\text{C}$ .

Tested extensively with deliberate liquid runouts

Hard-wired  $T_{\text{switch}}$  of 2 comparators by fixed resistor network.

# Typical Screen from Bridgeview User Interface Taken in I-Box Hysteresis Studies



I-box channel status

**Module Temperature Transients Provoked by  
Deliberate liquid run-out kept within acceptable  
limits (not exceeding +2 C) by I-Boxes**

# The I-Box and Thermal Runaway Prevention

- Silicon Detectors must be kept near  $-7\text{ C}$ .
- $I_{\text{leak}}$  and  $V_{\text{dep}}$  increase with irradiation over the lifetime of the detector.  $I_{\text{leak}}$  strongly temperature dependent and can cause a positive feedback runaway with  $T$ .

## **Low mass Requirement on cooling system**

**→→ LOW THERMAL MASS !!**

**At dissipation around 6 Watts/ detector tile,  
heat-up rates  $> 5\text{ C sec}^{-1}$  on Si,  
Evaporative OR Monophase liquid cooling!!!**

- Need fast, **HARD-WIRED** interlocks (DIGITAL) between temperature sensors on individual Si detectors & their individual multi-rail power supply channels  
( $> 6000$  in SCT & Pixel systems)
- Action **MUST NOT** depend on volatile SCADA software (PVSS2).  
(FPGA OK if on redundant, cascaded UPS, together with T Sensors & Discriminators)

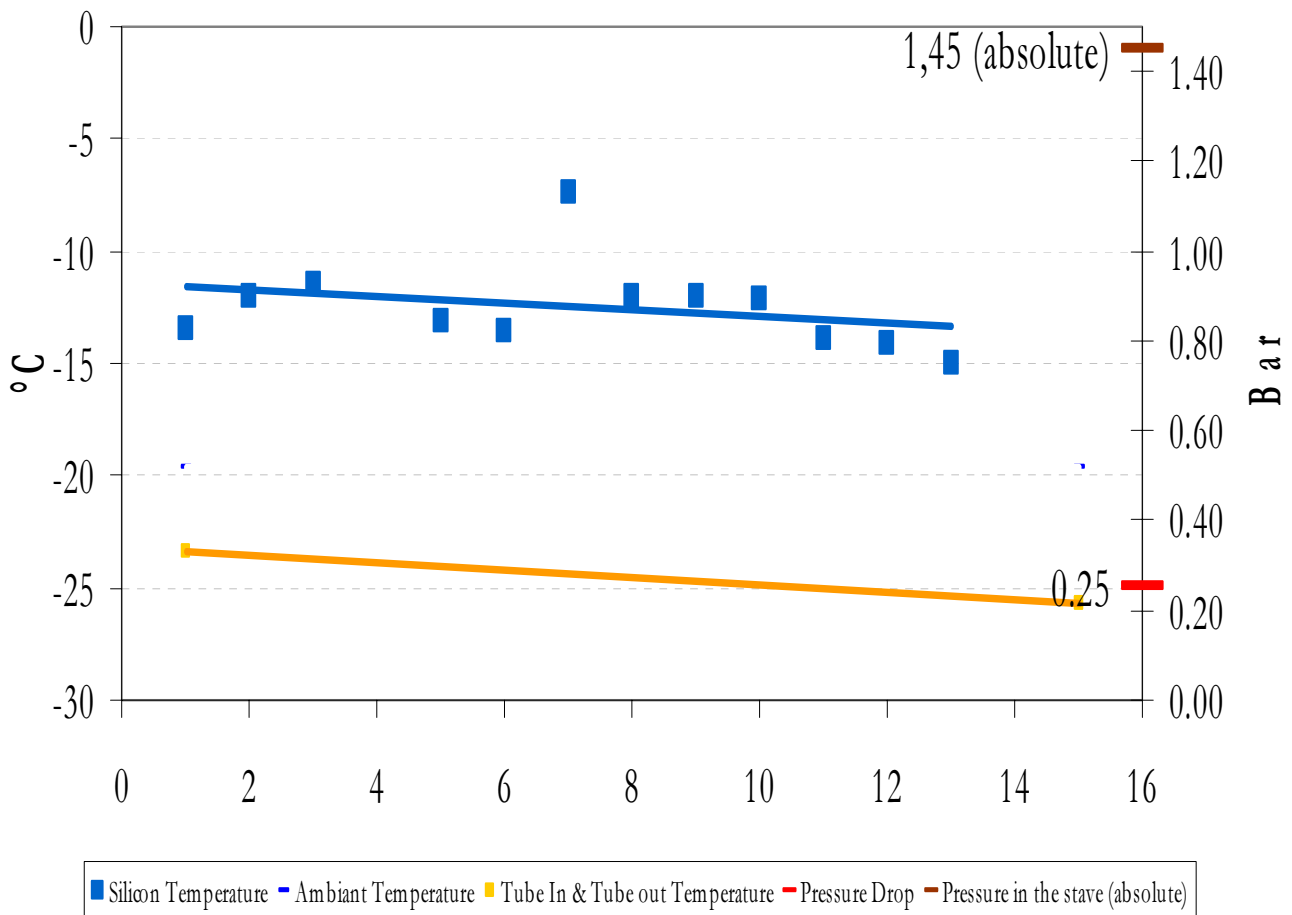
# Pixel Stave Re-Baselining Qualification

Stave thermal conduction test  
(November stave, After the Temperature cycles)

The Si temperature average is  $-12.96\text{ }^{\circ}\text{C}$  on the tilted Si,  
and  $-7.34\text{ }^{\circ}\text{C}$  on the middle Si.

The Pressure drop along the stave is  $0.2\text{ Bar}$ .

Thermal conduction after Thermal and pressure cycles  
(Power dissipated 134W)



# Flow and Pressure Control in the Evaporative Cooling System and Analog Pneumatic Controls Development

## EVAPORATIVE SYSTEM OPERATION

- Liquid refrigerant passes through injector / capillary at a mass flow rate dependent on the liquid pressure upstream of the injector
- Liquid refrigerant evaporates in the on-detector cooling channels with attached silicon detectors
- *Pressure in channel ==> evaporating temperature ==> silicon detector temperature*

- CONTROL PRINCIPLE

(Comparison vs. Liquid):

- Two Variable parameters

(1) Mass Flow Rate:

- pressure upstream of injector
- (via analog pneumatic-piloted regulator) ==>

(vs. pressure at start of liquid circuit)

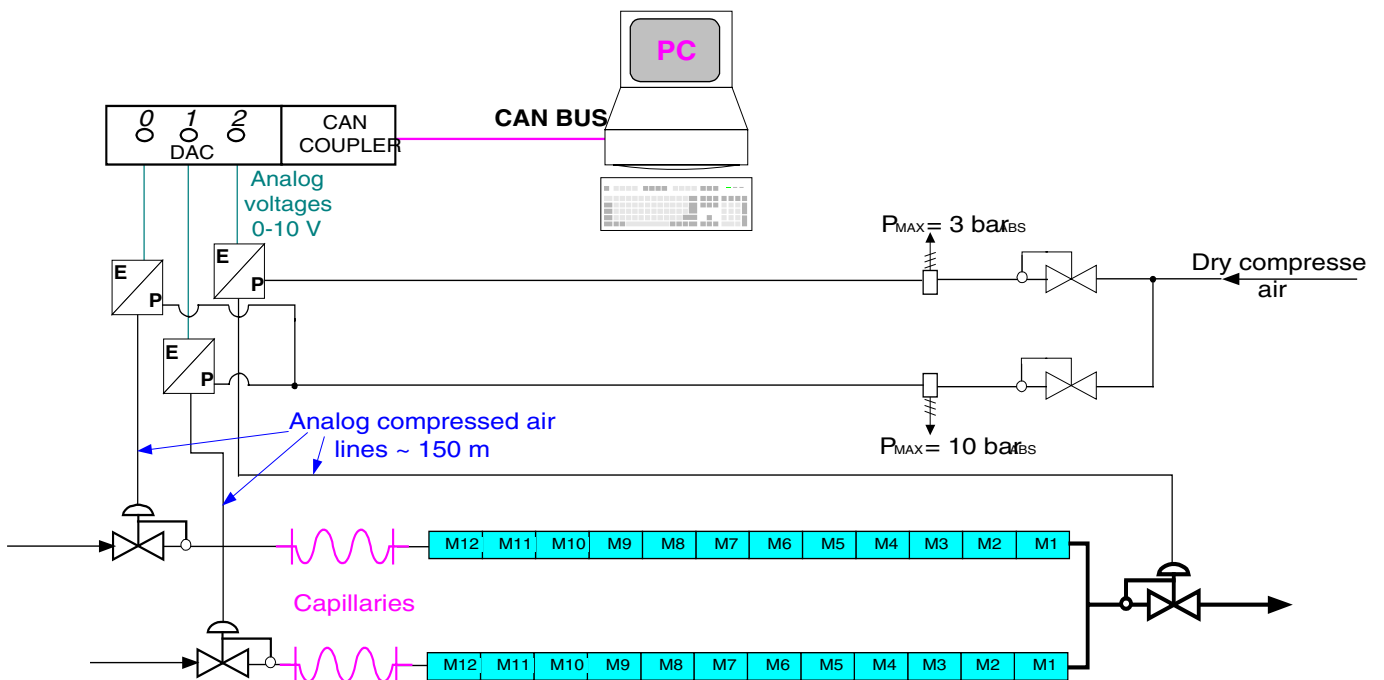
(2) Evaporating Temperature

- pressure in on detector cooling channel
- (via analog pneumatic-piloted back-pressure regulator) ==>

(vs. temperature of liquid delivery)

**INDIVIDUAL CIRCUIT TEMPERATURES NOT POSSIBLE IN PARALLEL LIQUID SYSTEM WITH SINGLE SUPPLY TEMPERATURE**

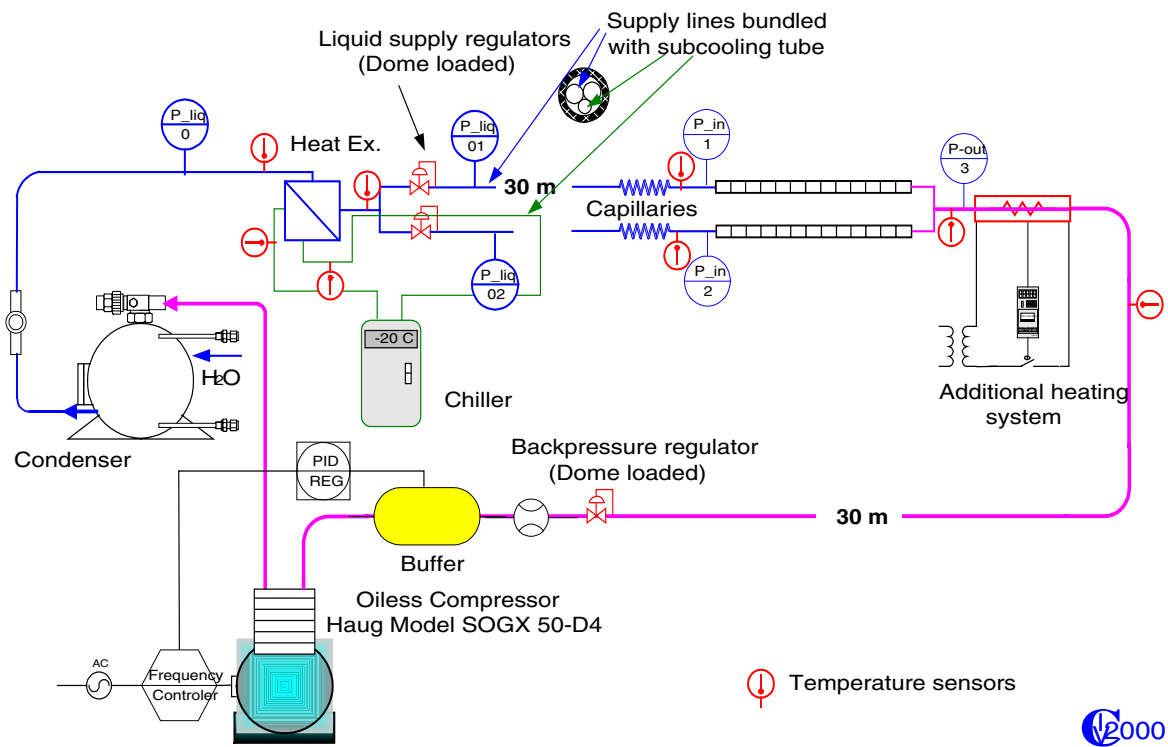
# Prototype Electro-Pneumatic Control Scheme





# Schematic of Prototype $C_3F_8$ Evaporative Recirculator

## Prototype Circulator and Control System



# FLOW VARIATION STUDIES

## (1) FLOW VARIATION VIA INTERLOCK “ON” BIT COUNTING

**DAC ➡ E2P ➡ Dome Loaded Regulator  
Pressure Upstream of Capillary ➡ Flow**

### PROTOCOL

$$P_{\text{CAPILLARY}} = P_{\text{SL}(T_{\text{in}})} + m * \# \text{ (powered modules)}$$

Where:  $P_{\text{SL}(T_{\text{in}})}$  is the saturated liquid pressure  
at the  $\text{C}_3\text{F}_8$  injection temperature (see cycle)  
 $m$  is incremental pressure (mbar)  
to remove heat of one Si module (~ 10 Watts)

**PROTOCOL DEMONSTRATED TO WORK:**  
(Temperatures on remaining powered modules and  
exhaust stable with varying flow/load)

**HOWEVER:** need first to *accurately* find  $m$  via;  
 $(P_{\text{CAPILLARY}(22 \text{ Modules})} - P_{\text{SL}(T_{\text{in}})})/22$

**ALSO, PROTOCOL sensitive to variable  
module power unless modified...**

$$P_{\text{CAPILLARY}} = P_{\text{SL}(T_{\text{in}})} + m' * \sum_i(\text{POWER}_{\text{module}(i)})$$

$m$  is normalized pressure/power factor (mbar/W),

**BUT...would need continuous V,I data for each  
module from DCS & Power Supplies: clumsy**

## Installed Test Structures and DAQ/Control System

Present status of the installation in the lab – part two

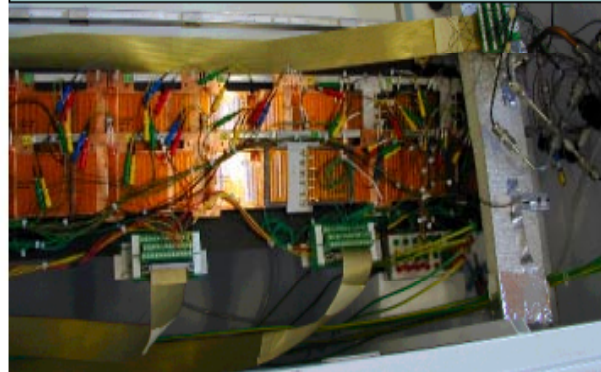


LMB and WAGO based  
CanBus DAQ System  
that enables monitoring of the  
temperatures and basic control  
parameters of the Cooling system



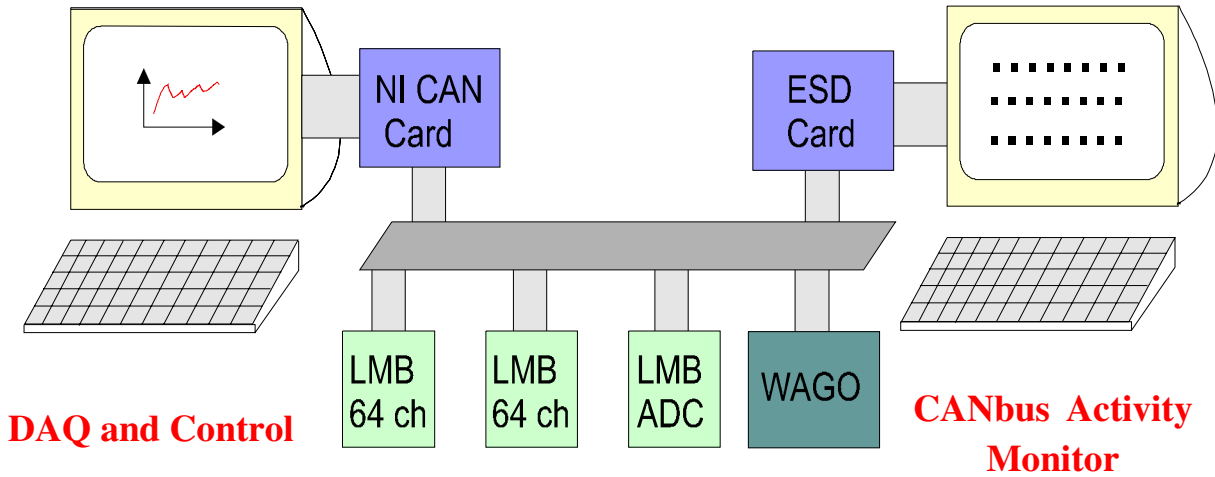
2 SCT thermal model staves and 2 "parallel ghost"  
SCT staves placed in the temperature controlled box

Detail of the manifolding into the staves,  
temperature sensors and heater wiring



©2000

# CAN-bus & LMB based measurement system



## CANbus Configuration

**LMB PT100:**  
(2 nodes)

**LMB ADC:**  
(4 nodes)

**WAGO:**  
(1 CAN coupler)

**Pressure (0-2.5V)**  
(8 Sensors)  
**Mass flow (0-2.5V)**  
(1 Sensor)

**Regulator Control**  
(Via E/P driver)  
(DAC 0-10V)  
(3 Channels)

**Temperature**  
**Pt-100, 4 wire**  
(64 Sensors)

**Temperature**  
**NTC (0-2.5V)**  
(32 sensors)

**Analyzer Heater**  
**Control**  
(DAC 0-10V)  
(1 Channel)

**Module Interlock**  
**Status (0-5V)**  
(32 sensors max)

# THE SOLUTION...

$C_3F_8$  proportional flow regulation to maintain Temperature

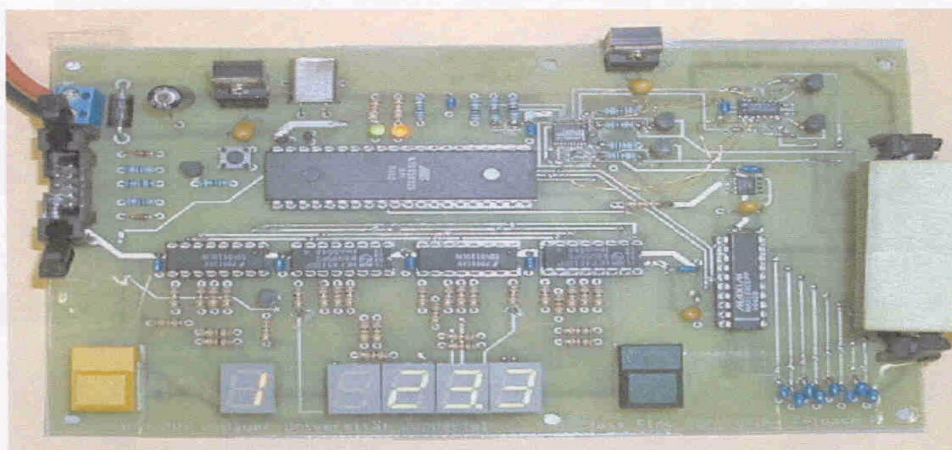
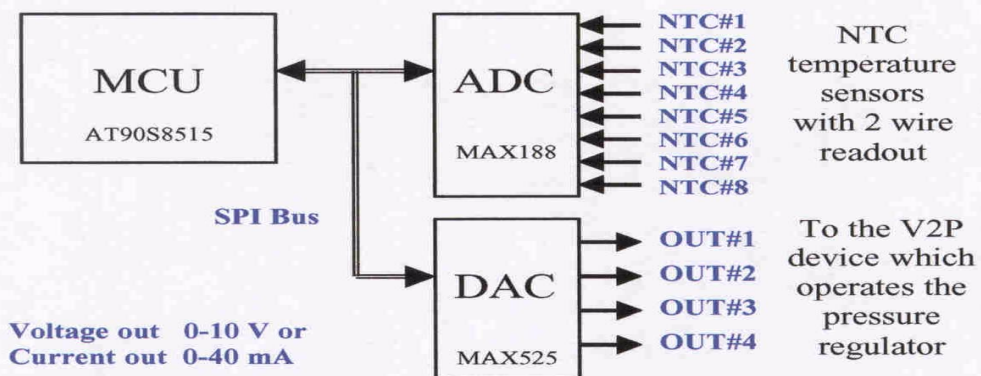
(NTC sensor) at exhaust above  $T_{evap}$  for varying (analog) load  
(Independent of module power variations)

## Single Chip PID For Coolant Flow Control (On ATMEL RISC $\mu$ Controller [C→Gnu])

Pixel Week at CERN

28 September 2000

### Schematic of the PID Controller



University of Wuppertal

## Functional description of the PID controller

- There can be up to 4 independent PID controllers in our prototype hardware.
- Each PID uses 2 temperature sensors: 1 main sensor [outlet tube, usually after the heater] and 1 security sensor [end of stave tubing].

Sample rate 4 Hz

$$\text{Out}_P = P * (\text{Temp} - \text{Setpoint})$$

$$\text{Out}_I = I * \text{Accumulated\_Error}$$

$$\text{Out}_D = D * (\text{Error} - \text{Last\_Error})$$

$$\text{Out} = \text{Out}_P + \text{Out}_I + \text{Out}_D$$

The temperature of the security sensor is monitored and if its value is above a defined critical temperature

$$\text{Temp}_{\text{crit}} = \text{Temp}_{\text{evap}} + \Delta\text{Temp}, \Delta\text{Temp} \in (2-3 \text{ K})$$

the PID mode is disabled. In this case a constant mass flow, capable of cooling the full staves power is used.

# All Hardware Elements of Cooling Control System Satisfactorily Demonstrated

- **Hard-wired Power Interlock & NTC sensors**
- **PID algorithm in ATMEL RISC  $\mu$** 
  - **DAC**
    - **V2P**
      - **Analog Air-loaded regulator for coolant flow control**
- **Powered modules and exhaust stable (in spec. ranges) during (1-22 module switching) transients and exhaust tube temperature maintained several degrees above evaporation temperature, indicating liquid run out maintained just beyond end of structure.**

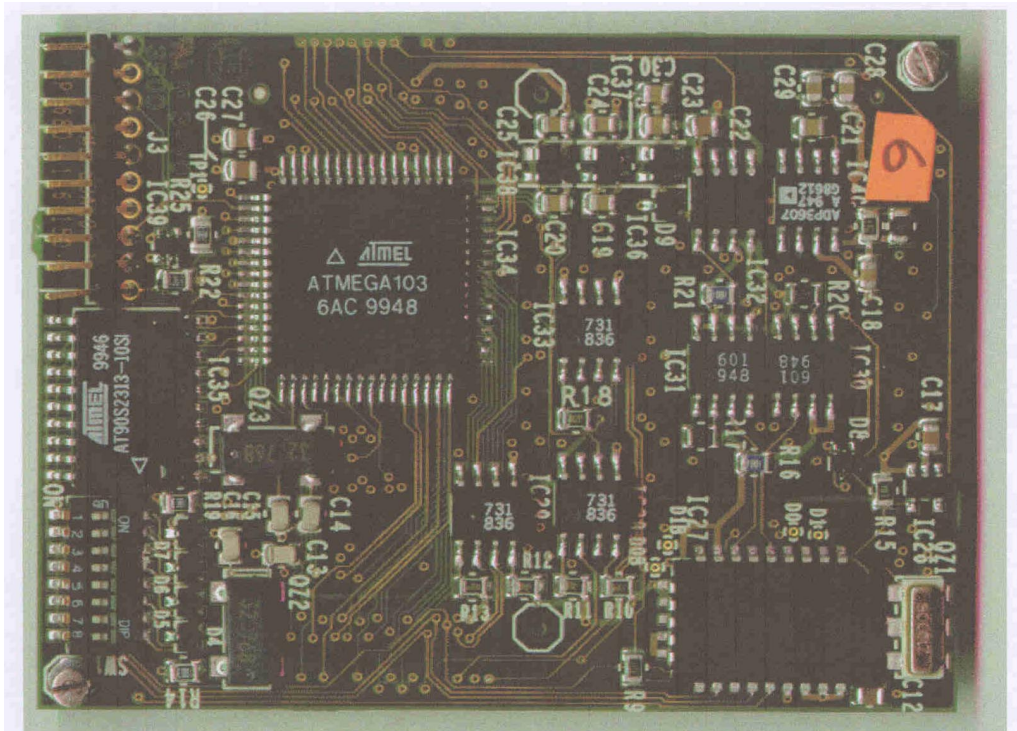
## † **Implications for Services**

- **With Flow regulation, unnecessary to directly heat individual exhaust tubes;**
- **With precooling of entry  $C_3F_8$  liquid, very low power required (ONLY!) on active insulation per circuit exhaust (~ 40W on 2 meters length, 5 mm Armaflex)**
- **Input Liquid Tubing Probably may not require active insulation with  $T_{precool} \sim -15^\circ C$  (to test).**

## **FUTURE STUDIES**

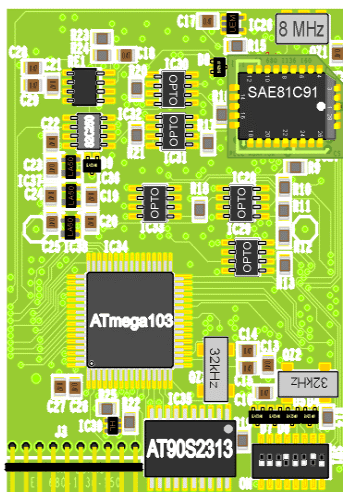
**Integrate the PID algorithm on new E-LMB, with new Development of Add-on DAC**

# Same ATMEL Family $\mu$ Controller in ATLAS DCS (E-Local Monitor Board)



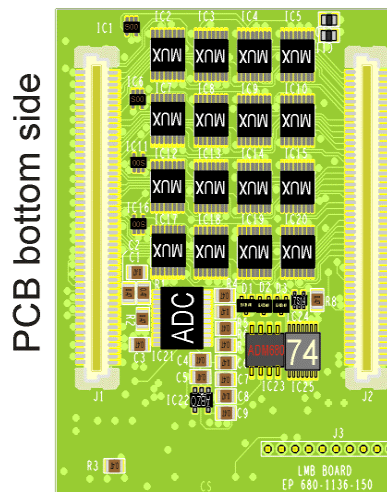
Front side of Embedded Local Monitor Board ELMB Size 50x66 mm October 2000 version

Top side



50x66mm

Bottom side



PCB bottom side

Optional ADC on the back side

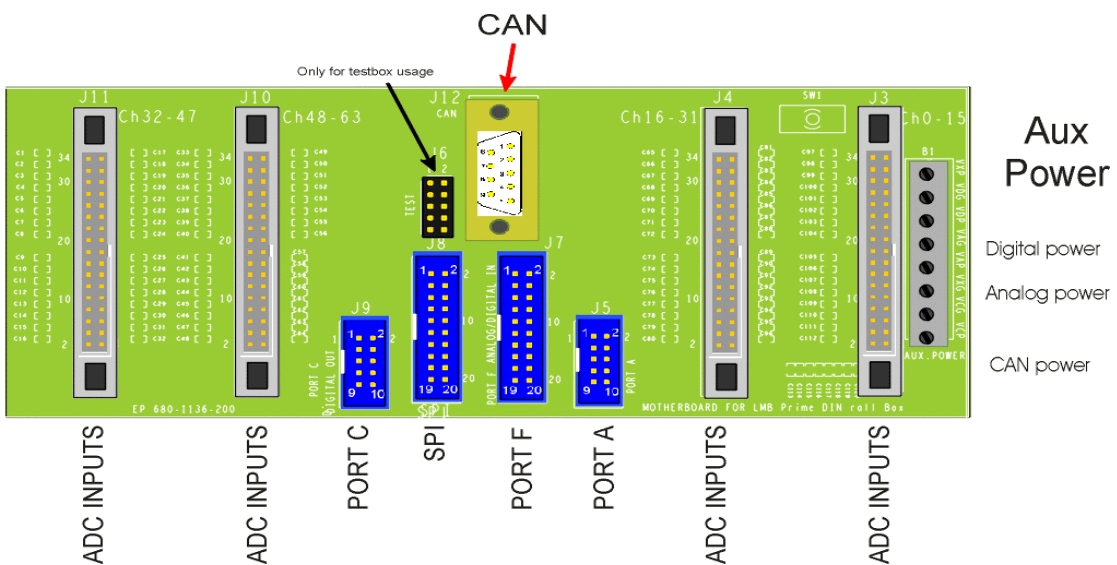
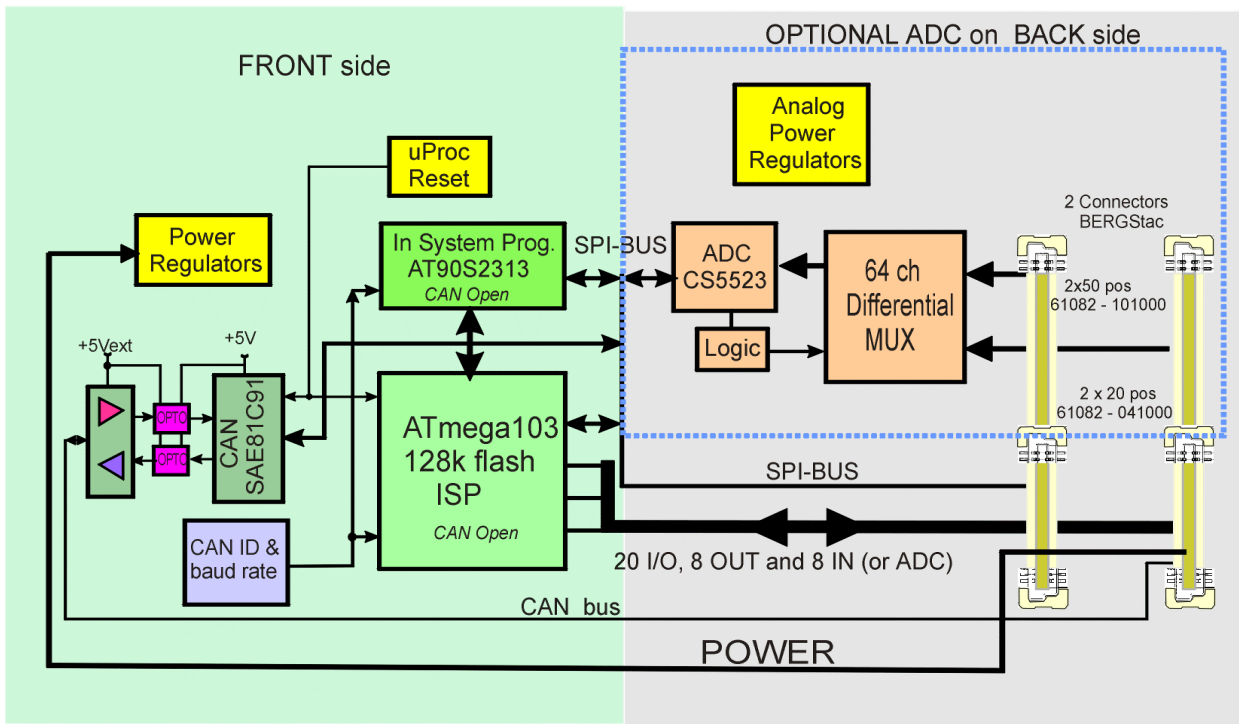
Mother board





# ATLAS E-LMB Block Diagram,

Shows ATMEL 128K RISC  $\mu$ Controller, SPI ports for connection to external DAC cards (NIKHEF)  
 ( $\mu$ controller allows flow control implementation using either smart (PID) algorithm, or else transparent (DAC only))



# Draft Specification for External E-LMB DAC

- (1) **Number of DACs per SPI port:** 4
- (2) **DAC Bits Precision :** 10\*

\* This precision sufficient for the pixel & SCT cooling controls (analog flow & evaporation pressure setting), but may be insufficient for other (as yet undefined) uses/users.

- (3) **E-LMB Connection Path:** SPI-PORT of E-LMB motherboard
- (4) **DAC Analog Output type:** 4-20 mA
- (5) **DAC Output connector:** 8-pin DIL ribbon (unshielded)
- (6) **Power Supply Rails:** As E-LMB/ motherboard
- Preference Compatibility with SPI-PORT (J8) on E-LMB motherboard viz: +5V analog, -5V analog, analog ground + 5V digital, digital ground
- (7) **Power Supply Connects:** Preferred via J8 (E-LMB motherboard SPI-PORT)
- (8) **Local Memory:** For 4 digital words (10 bit eqv.): one / DAC channel
- (9) **Time between local memory refresh:** 0.1 seconds minimum

# **Baseline Evaporative Circulator System**

## **In Personnel Accessible Area (USA 15)**

- **Remote, Hermetic, Oil-less compressors**
- **Local PID controllers regulating:**
  - aspiration pressure (compressor speed control)
  - condenser pressure (chilled water flow rate)
- **Six such compressor sets:**
  - Advantage of compressor parallelism:**  
**allows prior use in assembly sites.**

## **In Personnel Inaccessible area UX15**

**(high B, radiation fields)**

## **Dome Loaded Pressure Regulators for:**

### **Delivery of Sub-Cooled Liquid to each circuit**

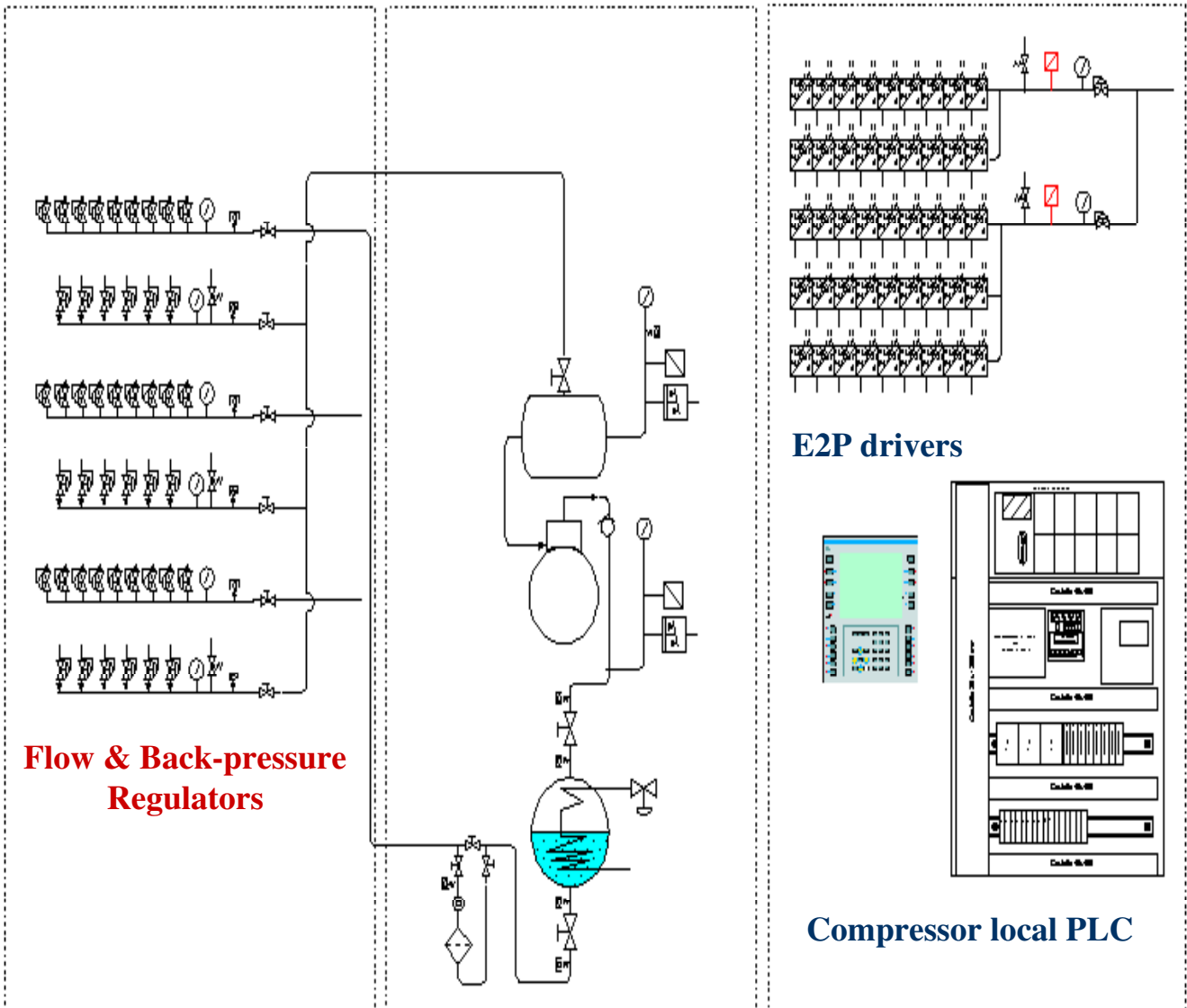
**(Linear Flow regulation between Condenser  
Pressure and Saturated Liquid Line)**

### **Operating temperature on each circuit,**

**control of boiling pressure  
(variable to accommodate Si radiation damage).**

### **Active Insulation on Critical Parts of Coolant Delivery and Exhaust Tubing**

# Placement of Recirculator Control Components in Final ATLAS Installation



**Regulators  
on ATLAS Service  
Platforms**

**Compressor, Condenser ,  
Compressor local PLC & E2P drivers  
in USA15 Technical Cavern**

# LMB (and I-Box) Channel Count for Pixel Modules

## (1) B-Layer

**NTCs for Module Count:  $12*13*2 = 312$ :**

**CORRESPONDING 64 Chan LMBs = 4.875**

**I-Box Channel Count:  $12*13*2 = 312$ :**

**Analog In Channel Count:  $12*13*2 = 312$  (I-Bit Status)**

**CORRESPONDING 64 Chan LMBs = 4.875**

## (2) Layer 1,2

**NTCs for Module Count:  $48*13*2 = 1248$ :**

**CORRESPONDING 64 Chan LMBs = 19.5**

**I-Box Channel Count:  $48*13*2 = 1248$ :**

**Analog In Channel Count:  $48*13*2 = 1248$  (I-Bit Status)**

**CORRESPONDING 64 Chan LMBs = 19.5**

## (3) Disks (Guess)

**NTCs for Module Count:  $26*6*4 = 624$ :**

**CORRESPONDING 64 Chan LMBs = 9.75**

**I-Box Channel Count:  $26*6*4 = 624$ :**

**Analog In Channel Count:  $26*6*4 = 624$  (I-Bit Status)**

**CORRESPONDING 64 Chan LMBs = 9.75**

**64 Chan LMBs (Modules Only) = 34.125**

**Additional 64 Chan LMBs (I-bits) = 34.125**

**THEREFORE COUNT I-BITS FOR FREE IN P/S?**

# LMB Channel Count for Pixel Coolant Monitor & Control

## (1) B-Layer (Example Breakdown)

**12 circuits of 2 staves in series: 12 inputs, 12 outputs**

**NTCS on/near on-detector structure per circuit (1/E-LMB analog input)**

- (1) Input, stave tube 1**
- (2) Output, stave tube 1 or Input, stave tube 2**
- (3) Output, stave tube 2 exhaust (control function)**
- (4) Output, stave tube 2 exhaust (reserve sensor for control function)**
- (5) Exhaust Remote (control function)**
- (6) Exhaust Remote (reserve sensor for control function)**
- (7) Pressure measurement (upstream of capillary)**
- (8) Pressure measurement (exhaust)**

**SUBTOTAL: 72 NTC sensors/ Analog Inputs**

**PID DACs in LMB  $\mu$ controllers for flow control:**

**(1/E-LMB analog output channel): 12**

**DACs in LMB  $\mu$ controllers for boiling pressure control:**

**(1/E-LMB analog output channel): 12**

**LMBs 1.125 (Analog Input Channels Only): 1.125**

**LMBs for DAC (@4 DAC/E-LMB): 6**

# LMB Channel Count for Pixel Coolant Monitor & Control

## (2) Layers 1,2 (Example Breakdown)

**48 circuits of 2 staves in series: 48 inputs, 48 outputs**

**NTCS on/near on-detector structure per circuit (1/E-LMB analog input)**

- (1) Input, stave tube 1**
- (2) Output, stave tube 1 or Input, stave tube 2**
- (3) Output, stave tube 2 exhaust (control function)**
- (4) Output, stave tube 2 exhaust (reserve sensor for control function)**
- (5) Exhaust Remote (control function)**
- (6) Exhaust Remote (reserve sensor for control function)**
- (7) Pressure measurement (upstream of capillary)**
- (8) Pressure measurement (exhaust)**

**SUBTOTAL: 368 NTC sensors/ Analog Inputs**

**PID DACs in LMB  $\mu$ controllers for flow control:**

**(1/E-LMB analog output channel): 48**

**DACs in LMB  $\mu$ controllers for boiling pressure control:**

**(1/E-LMB analog output channel): 48**

**LMBs 1.125 (Analog Input Channels Only): 5.75**

**LMBs for DAC (@4 DAC/E-LMB): 24**

# LMB Channel Count for Pixel Coolant Monitor & Control

## (3) Disks (Example Breakdown)

**26 circuits of multisectors in series: 26 inputs, 26 outputs**

**NTCS on/near on-detector structure per circuit (1/E-LMB analog input)**

- (1) Input, stave tube 1**
- (2) Output, stave tube 1 or Input, stave tube 2**
- (3) Output, stave tube 2 exhaust (control function)**
- (4) Output, stave tube 2 exhaust (reserve sensor for control function)**
- (5) Exhaust Remote (control function)**
- (6) Exhaust Remote (reserve sensor for control function)**
- (7) Pressure measurement (upstream of capillary)**
- (8) Pressure measurement (exhaust)**

**SUBTOTAL: 208 NTC sensors/ Analog Inputs**

**PID DACs in LMB  $\mu$ controllers for flow control:**

**(1/E-LMB analog output channel): 26**

**DACs in LMB  $\mu$ controllers for boiling pressure control:**

**(1/E-LMB analog output channel): 26**

**LMBs 1.125 (Analog Input Channels Only): 3.25**

**LMBs for DAC (@4 DAC/E-LMB): 13**



# LMB Channel Count for Pixel Tube Bundle External Temperature Control

## Assumption:

Each bundle has active insulation over ~30 m between PPB3 & PPB1, which is divided into 3 zones as follows :

- (1) PPB1 to end of ID volume
- (2) End of ID volume to PPB2
- (3) PPB2 to PPB3

Each zone of each bundle has 4 temperature sensors :  
2 for monitoring and 2 for control:

Two require PID activity to control the active insulation heaters.

Surface	Input Bundles / End	Output Bundles /End	Totals (Both Ends)
<b>B layer</b>	<b>4(3 tubes)</b>	<b>4(3 tubes)</b>	<b>8 (3 tubes)</b>
<b>1,2</b>	<b>4(6 tubes)</b>	<b>8(3 tubes)</b>	<b>24</b>
<b>Disks</b>	<b>1(6 tubes)</b>	<b>3(3 tubes)</b>	
	<b>1(7 tubes)</b>	<b>1(4 tubes)</b>	<b>12</b>
<b>Total No bundles (Both ends):</b>			<b>44</b>
<b>No Zones (44*3) :</b>			<b>132</b>
<b>No Sensors (44*3*4) :</b>			<b>528</b>
<b>E-LMBs for these Sensors :</b>			<b>8.25</b>
<b>No PID controllers (44*3) :</b>			<b>132</b>
<b>E-LMBs for PID controllers:</b>			<b>33</b>

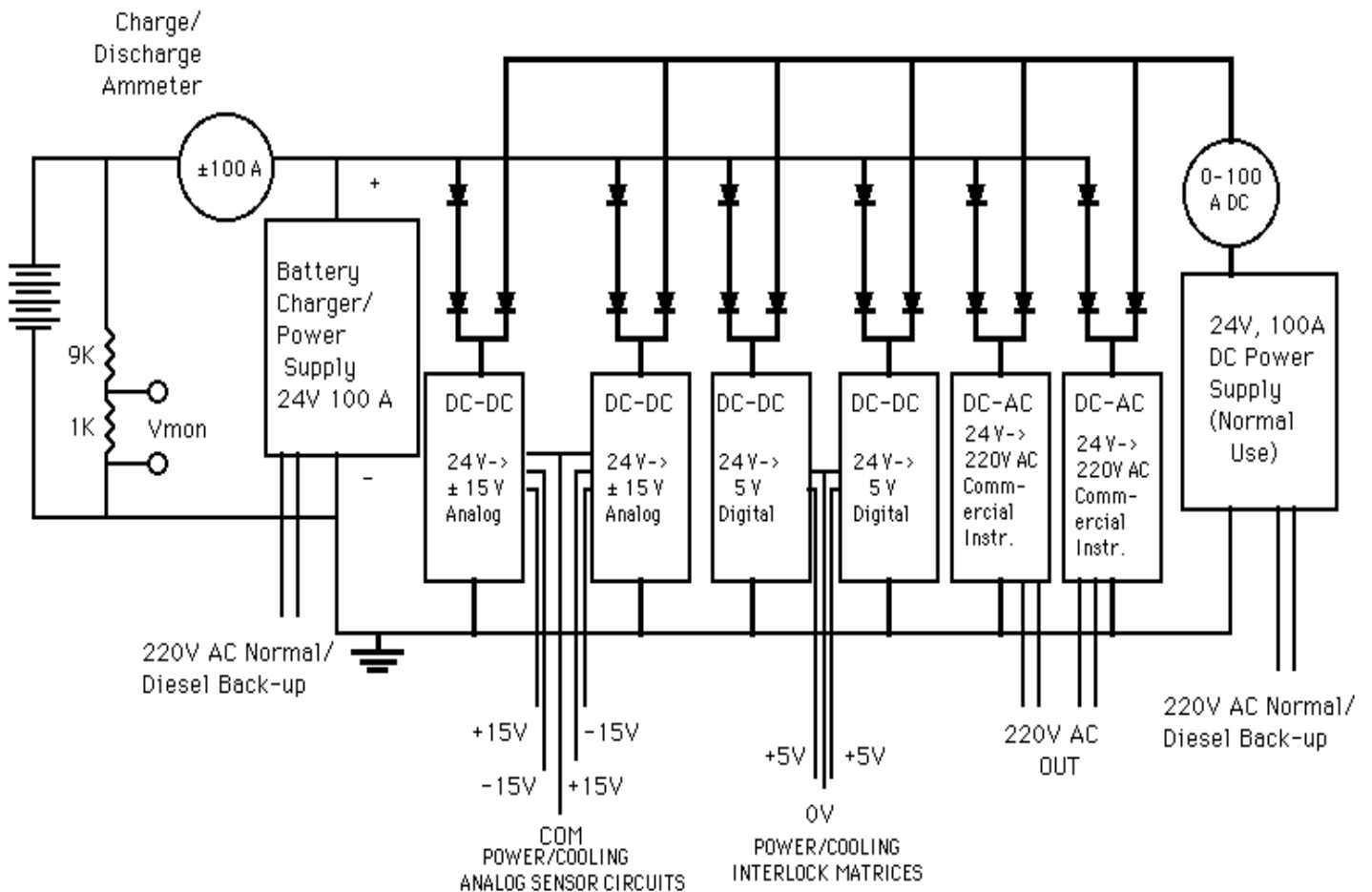
**TOTAL E-LMB REQUIREMENT (SET & SUBSET):**  
**(MODULES+CIRCUIT CONTROL+TUBE BUNDLES)**  
**52.5 (INPUTS, NOT INCLUDING I-Bits, 76 for DAC/PID DAC)**

## CONCLUDE:

**NEED 8 PID DACs PER E-LMB, OR REDUCE # BUNDLE ZONES)**

# Highly Redundant UPS for I-Box Power

- **Most Commercial UPS gives 120/220V, generated by DC-AC conversion, OK for servers etc...**
  - **Protects against primary AC failure and lightning etc but does not protect against downstream AC-DC supply failure.**
- **It is preferable to have the redundancy as close as possible to the protected load: i.e. at the LVDC level**



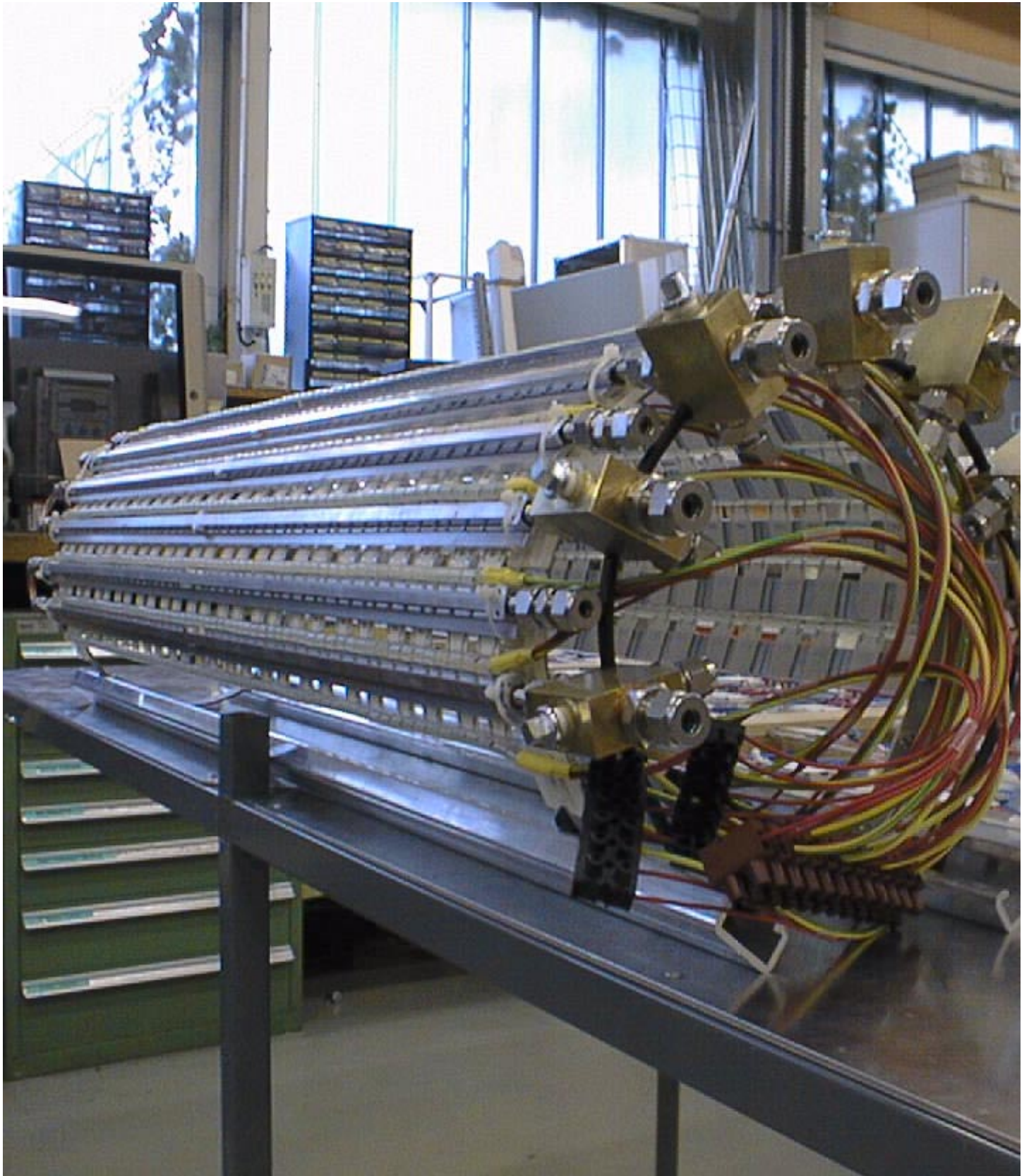
**we need now to start development:**

**Candidate DC-DC converters include Kepco ERD series.**

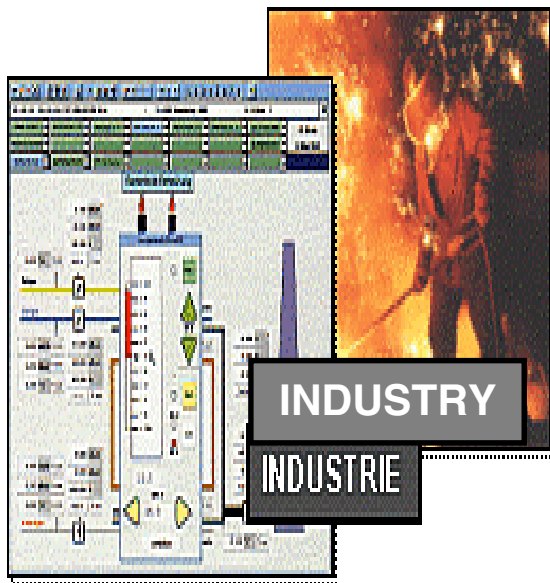
## Modularity of Circuits and Analog Flow Elements in ATLAS SCT & Pixel Evaporative Cooling Demonstrator.

Layer	Circuits	Supply Capillaries / Circuit	Power/ (Output) circuit (W)	Flow regs	Boiling Pr. Regs
SCT 4	2	2	480	4	2
SCT 3	2	2	480	4	2
SCT 2	2	1	480	2	1
SCT 1	2	1	480	2	1
Pixel 2	3	1	208	3	3
Pixel 1	2	1	208	2	2
B layer	1	1	288	1	1
SCT disk/4	1	3	330	3	1
Pixel disk/6	1	1	96	1	1
<b>TOTALS</b>			<b>4218</b>	<b>22</b>	<b>14</b>
<b>TOTAL FOR SCT 4</b>			<b>6720</b>	<b>28</b>	<b>14</b>

# Dummy Pixel Staves for Cooling Demonstrator



# ATLAS SCADA: PVSS2. Chosen 9/2000 Until 6/2001 for Evaluation/Final Decision: Range of Application



**INDUSTRY**  
**INDUSTRIE**



**ENERGY & AIR  
CONDITION**

**PVSS II**

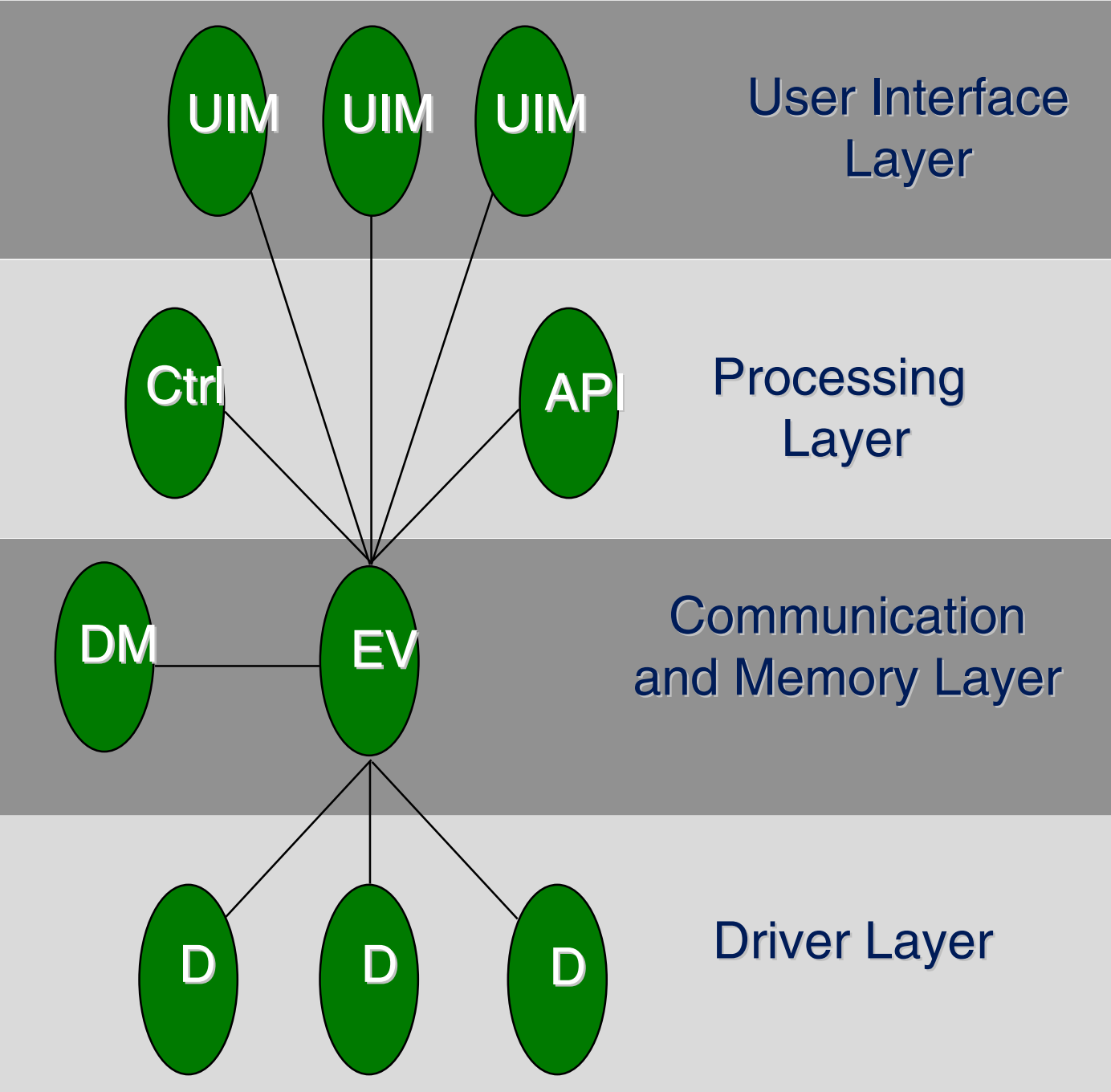


**ENVIROMENT**



**TRAFFIC CONTROL**

# PVSS II Manager Overview



# System management / user admin.

The screenshot shows the 'Vision\_9: system management' application window. In the foreground, the 'PVSS: User Administration' dialog box is open. The dialog has a menu bar with 'File', 'Panel', and '?'. Below the menu bar are icons for file operations and a help icon. The main area of the dialog is divided into several sections:

- Users:** A table listing users and their properties.
- Groups & authorization:** Buttons for 'Group administration...', 'Authorization levels...', and 'Workstation authorization...'.
- Users:** Buttons for 'Add user...', 'Change user...', and 'Delete user...'.
- Authorization levels:** Two columns of checkboxes for 'Authorization levels:' and 'Independent of the workstation:'.
- Buttons:** 'Help' and 'Close' buttons at the bottom right.

The 'Users' table contains the following data:

User name	Group	ID	User language
root	root	0	de_AT.iso88591
para	para	0	de_AT.iso88591
operatorAll	operatorAll	0	de_AT.iso88591
operator	operator	0	de_AT.iso88591
guest	guest	0	de_AT.iso88591
gast	guest	1	de_AT.iso88591
demo	guest	2	en_GB.iso88591

The 'Authorization levels' section shows two columns of checkboxes, numbered 1 through 11. The 'Authorization levels:' column has all checkboxes checked, while the 'Independent of the workstation:' column has all checkboxes unchecked.

At the bottom left of the dialog, the text 'current user: root' is displayed.



# Alert class

Vision\_1: data point parameter

File Panel ?

filter options:  
 internal datapoints

dp-filter:

- ExampleDP\_Int
- ExampleDP\_Text
- valve
- valve1
- valve2
- valve1\_1
- common
- lock
- defaults
- response
- common
- lock
- 5.4 opening
- 01 opened
- 01 closed
- 01 engine runs
- 01 malfunction
- original
- alert class
- common
- dp\_fct
- lock
- valve2\_1
- valve1\_2
- valve2\_2

### DP-Parameterization

#### Alert class

DPE: System1:valve1\_1.response.malfunction

Alert parameters Arguments

alert priority: 10 short sign: W  acknowledging author: 0

save alerts

requires individual ack.  acknowledge old alerts

acknowl. type: Pair of alerts must be acknowledged

Alert status	Alert color	Alerting
no alert	Original color	
CAME/unacknowl.	<[0,80,100],2,Weiss,2,[100,100	
CAME/acknowl.	[0,80,100]	
WENT/unacknowl.	<[0,60,0],3,Weiss,3,[100,100,10	
K/G/unacknowl.		

OK Cancel Apply Help

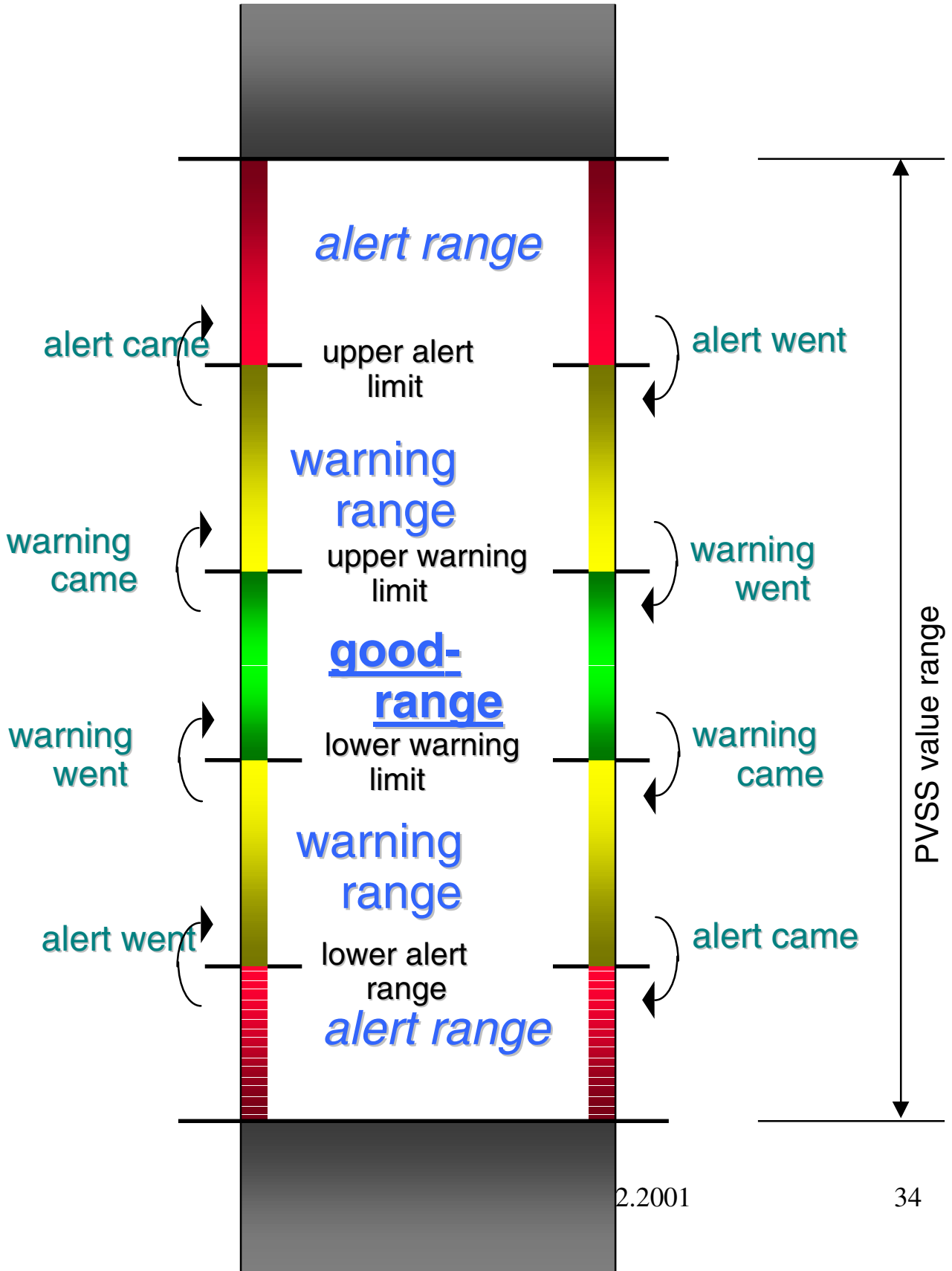


# PVSS II Uses C-like Scripts to Link DataPoints (eg analog inputs like T, P) to communicate with DB, reactions: Example for a Ctrl-Function

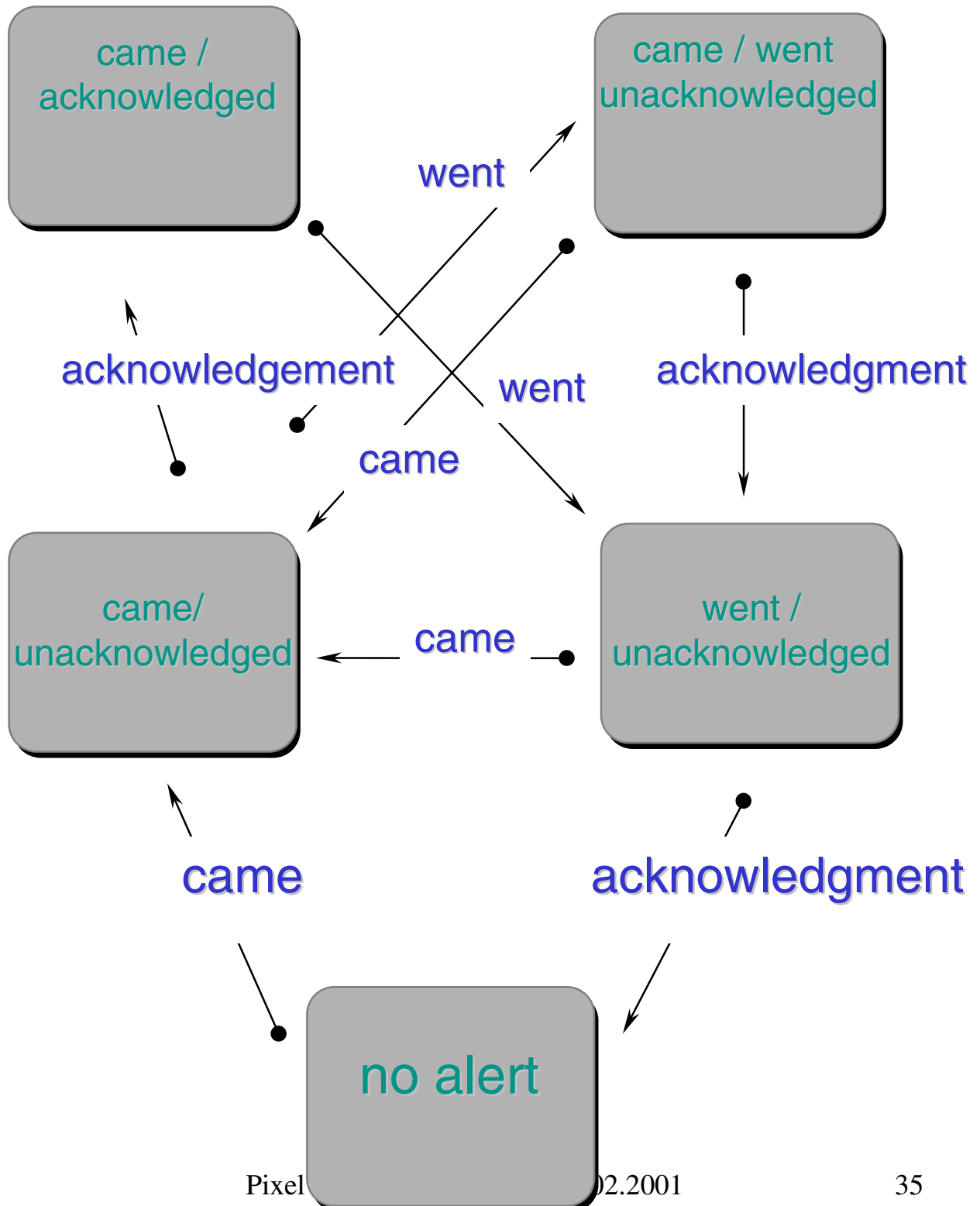
```
workCB (string dp, int x, int y)
{
    int z;

    z = x + y;
    dpSet(dp, z); /* writes the value
of "z" to the data-point "dp" */
}
```

# Definitions



# PVSS II „Came“ and „Went Alarms Require and Log Acknowledgements



# DCS DAQ Electronics Status

- **First pre-production E-LMBs delivered**
  - (In pixels, CERN, Wuppertal have taken delivery)
- **Small E-LMB test system running with PVSS II SCADA software in cooling lab**
- **Requested 25 E-LMBs (delivery Spring '01) for Evaporative Cooling Demonstrator and Cooling System at SCT assembly site #1 (Oxford, late '01)**
- **Scalable PVSS2 with E-LMB system to be developed for Evaporative Cooling Demonstrator (2 students, end Feb + V. Filimonov for 2 months)**
- **Need to speed Add-On DAC development for E-LMB SPI Bus (Wuppertal/ NIKHEF)  
Convergence to common ATLAS spec has started**
- **Experience has shown Cooling Developments are best motor for controls/ DCS DAQ development:**
- **PVSS2+E-LMBs at Local Site when pixel cooling tests shift from CERN?? (Much to do...)**

# SOME FAULT RESPONSE ACTIONS

FROM SAFETY ANALYSIS REPORT JUNE 2000, CONTACT: G. BENINCASA

## (1) Global LVDC power failure

**Need to protect structures from excessive cold at 0 power.**

→ → Taken care of within a few seconds by analog flow regulation scheme on the basis of sensed exhaust temperature. (See later in talk)

## (2) Isolation of a Cooling Circuit

**Prevent excessive pressure building up in inactive circuit containing C<sub>3</sub>F<sub>8</sub> liquid valves/regulators.**

→ → First close C<sub>3</sub>F<sub>8</sub> liquid supply regulator  
(Analog compressed air signal #1 via I→P  
to Saturated Liquid Pressure or below)

**NOTE: Exhaust back-pressure regulator NOT a shut-off device:**

→ → will regulate C<sub>3</sub>F<sub>8</sub> boiling pressure  
to its dome load pressure  
(analog compressed air signal #2 via I→P)

## (3) Turn-on to correct boiling pressure.

**Compressor Aspiration Tank pre-filled to preferred pressure (P<sub>tank</sub> > P<sub>evap</sub>) with superheated C<sub>3</sub>F<sub>8</sub> vapor (via flash evaporation from liquid delivery), for start of pressure ramp down**

→ → then reduced at required speed  
(analog air signal #2 to back-pressure regulator)

## (4) DACs, I→P Regulators MUST be on Cascaded Redundant UPS.